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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/830,019	04/23/2004	Yoshiki Kashiwagi	042264-0101	7656

22428 7590 12/20/2005

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EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/830,019	KASHIWAGI ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	TT

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 04/23/2004. Claims 1-13 are pending.

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The disclosure is objected to because of the following informalities: in the specification, on page 6, ll. 11-14 (see " according to claim 1") and on page 7, ll. 1-3 (see "according to claim10"), the specification does not contain adequate written description of the invention application. On page 12, ll. 14, the "short-through current" appears to be an error (see " shoot-through current" in the specification, col. 12, ll. 4-5, ll. 9, and ll. 19).

Appropriate correction is required.

3. **Claims 2** is objected to because of in line 3, the recited "short-through current" appeared to be an error (see " shoot-through current" in the specification, col. 12, ll. 4-5, ll. 9, and ll. 19). Appropriate correction is required.

4. **Claims 2-8** are objected to because of the following informalities: the "A" in the phrase " A method of designing a semiconductor circuit device according to ..." recited in the claims should be replaced with the word "The" . Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any

> person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. **Claim 3** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

7. **Claim 3** is rejected to because of the limitation in claim 3 is not fully described in the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. **Claims 1, 5, and 7-13** are rejected under 35 U.S.C. 102(e) as being anticipated by Fukasawa (US Patent No. 6941534).

Referring to claim 1 and similarly recited claims 10 and 13, Fukasawa discloses a method of designing a semiconductor circuit device, comprising the steps of:

generating first circuit data comprising information on a first circuit

driven by a voltage from a first power system (col. 2, ll. 59 through col. 4, ll. 12, see the " first standard cell");

generating second circuit data comprising information on a second circuit driven by a voltage from a second power system different from the first power system (col. 2, ll. 59 through col. 4, ll. 12, see the " second standard cell");

obtaining cell data prestored in a storage medium and comprising information on a boundary circuit (col. 2, ll. 59 through col. 4, ll. 12); and

generating boundary circuit connection information indicating that the boundary circuit is connected on a transmission path between the first circuit and the second circuit (col. 2, ll. 59 through col. 4, ll. 12, see the " level converter cell");

Referring to claim 5, Fukasawa discloses the method of designing a semiconductor circuit device according to claim 1, wherein the boundary circuit comprises a circuit for level conversion between the first circuit and the second circuit (*col. 2, ll. 59 through col. 4, ll. 12, see the " level converter cell").*

Referring to claim 7, Fukasawa discloses the method of designing a semiconductor circuit device according to claim 1, wherein the first circuit data, the second circuit data, and the cell data are data for logic circuit design (col. 1, ll. 6-11; col. 6, ll. 37-54).

Referring to claim 8, Fukasawa discloses the method of designing a semiconductor circuit device according to claim 1, wherein the first circuit data, the second circuit data, and the cell data are data for layout design (col. 1, ll. 6-11; col. 3, ll. 22-24 and 50-53).

Referring to claim 9 and similarly recited claim 11, Fukasawa discloses the semiconductor circuit device designed by a method of designing a semiconductor circuit device according to claim 1 (in abstract, col. 2, ll. 59- col3, ll. 6, see a first standard cell (" a first circuit"), a second standard cell (" a second circuit"), and a level converter cell (" boundary circuit").

Referring to claim 12, Fukasawa discloses a computer-readable storage medium for storing a cell library used for semiconductor design, comprising:

a boundary cell comprising information on a boundary circuit connected on a signal transmission path between a first circuit driven by a voltage from a first power system and a second circuit driven by a voltage from a second power system different from the first power system (col. 3, ll. 50 through col. 4, ll. 12; Fig. 9-10; col. 7, ll. 47 through col. 9, ll. 35, see level converter cell("boundary cell") and storage medium 59).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 2-4, and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukazawa (US Patent No. 6941534) in view of Toyama et al. (US Pat. No. 6603219).

Referring to claim 2, Fukazawa discloses substantially all the elements in claim 1 except wherein the boundary circuit comprises a circuit for suppressing

short-through current between the first circuit and the second circuit when one of the first circuit and the second circuit is off and another one of the first circuit and the second circuit is on.

Toyama et al. discloses power supply control circuits (in Fig. 2-3, elements 2 and 5; col. 3, ll. 47 through col. 5, ll. 47) that are used to suppress a shoot-through current in an active circuit area while the other circuit area is inactive (col. 3, ll. 47 through col. 5, ll. 47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of Fukazawa with the method disclosed by Toyoma et al. because such modification includes a shoot-through current suppression circuit for the boundary cell would have been used to eliminate the shoot-through current when one circuit is "on" and the other is "off", to thereby "providing a semiconductor IC device having a function selecting circuit operable at a high level of reliability while consume low power" (col. 2, ll. 35-38).

Referring to claim 3, Fukazawa discloses substantially all the elements in claim 1 except wherein the boundary circuit comprises a circuit for preventing circuit malfunction due to indeterminate current between the first circuit and the second circuit when one of the first circuit and the second circuit is off and another one of the first circuit and the second circuit is on .

Toyama et al. discloses power supply control circuits (in Fig. 2-3, elements 2 and 5; col. 3, ll. 47 through col. 5, ll. 47) that are used to prevent a malfunctioning in an inactive circuit while the other circuit is inactive (col. 3, ll. 47 through col. 5, ll. 47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of Fukazawa with the method disclosed by Toyoma et al. because such modification includes a circuit for preventing circuit malfunction would have been used to prevent the undesirably malfunctioning of the inactive circuit while the other circuit is active (col. 5, ll. 5-14), to thereby "providing a semiconductor IC device having a function selecting circuit operable at a high level of reliability while consume low power" (col. 2, ll. 35-38).

12. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukazawa (US Patent No. 6,941,534) in view of Hirata et al. (US Pat. No. 6,140,864).

Fukazawa discloses substantially all the elements in claim 1 except wherein the boundary circuit comprises a circuit for suppressing leakage current between the first circuit and the second circuit when one of the first circuit and the second circuit is off, and another one of the first circuit and the second circuit is on.

Hirata et al. disclose a circuit (Fig.1, circuit block 20) that can be used to reduce/suppress a leakage current in an LSI circuit. The circuit composed of an AND gate and inverters connected in cascade. The circuit is switchable between an active state and a standby state by a chip activate signal CS (col. 3, ll. 11-52).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of Fukazawa with the method disclosed by Hirata et al. because such modification includes a leakage current suppression circuitry for the boundary cell would have been used to reduce the leakage current in the semiconductor circuit, to thereby providing reduction in the power

consumption of the circuit block in the standby state (see abstract; col. 2, ll. 11-21).

13. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukazawa (US Patent No. 6941534) in view of Voldman (US Pat. No. 5610791).

Fukazawa discloses substantially all the elements in claim 1 except wherein the boundary circuit comprises a protection circuit for protecting a transistor in the first circuit and/or the second circuit from electrostatic discharge.

Voldman discloses a design of electrostatic discharge (ESD) protection circuitry that is used to suppress the ESD in IC chips having multiple power supply rails (col. 3, ll. 62 through col. 4, ll. 38; in fig. 3, elements11, 13, and 15). The ESD protection circuit taught by Voldman can prevent a current flow from an energized rail/circuit to a de-energized rail/circuit that can cause a short circuit (col. 1, ll. 60 through col. 2, ll. 17). The short circuit between the two power rails can damage circuit components such as transistors in the circuits that connected to the power rails.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of Fukazawa with the method disclosed by Voldman because such modification includes a ESD protection circuitry for the boundary cell would have been used to protect the circuits from the ESD, to thereby providing a " power sequence independent" ESD protection circuits for the circuits that connected to the power rails (col. 4, ll. 10-17).

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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